to a crystal plane on which the growth rate of the first semiconductor is substantially zero.

6. *(Twice Amended)* A transistor according to claim 1 wherein the conducting means comprises an elongate region of the first semiconductor in a bottom region of the second semiconductor, that is in a bottom region of the lined groove.

C7

8. *(Twice Amended)* A transistor according to claim 1 wherein said at least one elongate conducting means comprises two elongate conducting means.

C8

12. *(Twice Amended)* A transistor according to claim 1 wherein said at least one further electrode is arranged to provide confinement in a third dimension for charge carriers within the conducting means, in which hard confinement in two dimensions holds charge carriers within the conducting means.

C9

13. *(Twice Amended)* A transistor according to claim 1 wherein said at least one further electrode is arranged substantially transverse to the conducting means.

14. *(Twice Amended)* A transistor according to claim 1 wherein said at least one further electrode is arranged to cause a peak within the energy bands of the first semiconductor of the conducting means.